module tb\_phase\_1;

reg clk;

reg reset;

reg enable;

reg code\_in;

wire phase\_1done;

phase\_1 dut(.clk(clk),.reset(reset),.enable(enable),.code\_in(code\_in),.phase\_1done(phase\_1done));

initial clk=0;

always #5 clk=~clk;

initial begin

reset=0;

code\_in=0;

enable = 1;

#20 reset=1;

#10 code\_in=1;

#10 code\_in=0;

#10 code\_in=1;

#10 code\_in=1;

#10 code\_in=0;

#50;

$finish;

end

endmodule